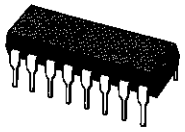
SGS-THOMSON MICROELECTRONICS

M74HCT7259

8 BIT ADDRESSABLE LATCH/DECODER/RELAIS DRIVER (OPEN DRAIN, INVERTING OUTPUT)

- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  90 LSTTL LOADS
- HIGH CURRENT OPEN DRAIN OUTPUT UP TO 80 mA



B1R
(Plastic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :
M74HCT7259B1R M74HCT7259M1R
M74HCT7259C1R

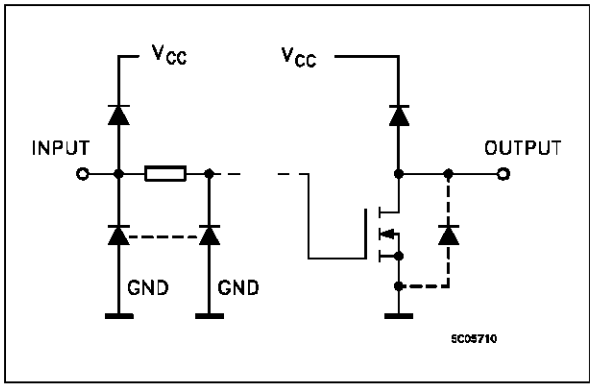
DESCRIPTION

The **M74HCT7259** is a high speed CMOS 8 BIT ADDRESSABLE LATCH/DECODER fabricated in silicon gate C2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

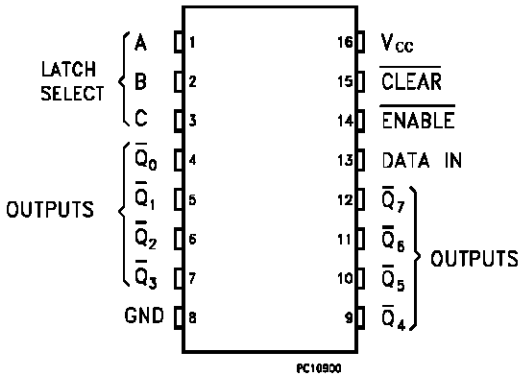
The **M74HCT7259** has single data input (D) 8 LATCH inverted OUTPUTS ($\overline{Q0}$-$\overline{Q7}$), 3 address inputs (A, B and C), common enable input ($\overline{ENABLE}$) and a common $\overline{CLEAR}$ input. To operate this device as an addressable latch, data is held on the D input, and the address of the latch into which the data is to be entered is held on the A, B and C inputs.

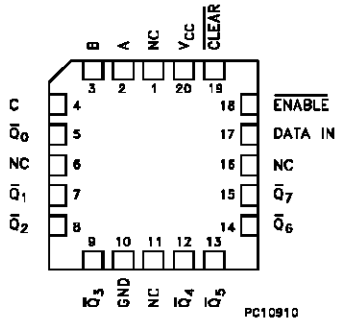
When $\overline{ENABLE}$ is taken low the data flows through to the address output. The data is stored on the positive-going edge of the $\overline{ENABLE}$ pulse. All unadressed latches will remain unaffected. With $\overline{ENABLE}$ in the high state the device is deselected and all latches remain in their previous state, unaffected by changes on the data or address inputs. To eliminate the possibility of entering erroneous data into the latches, the $\overline{ENABLE}$ should be held high

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



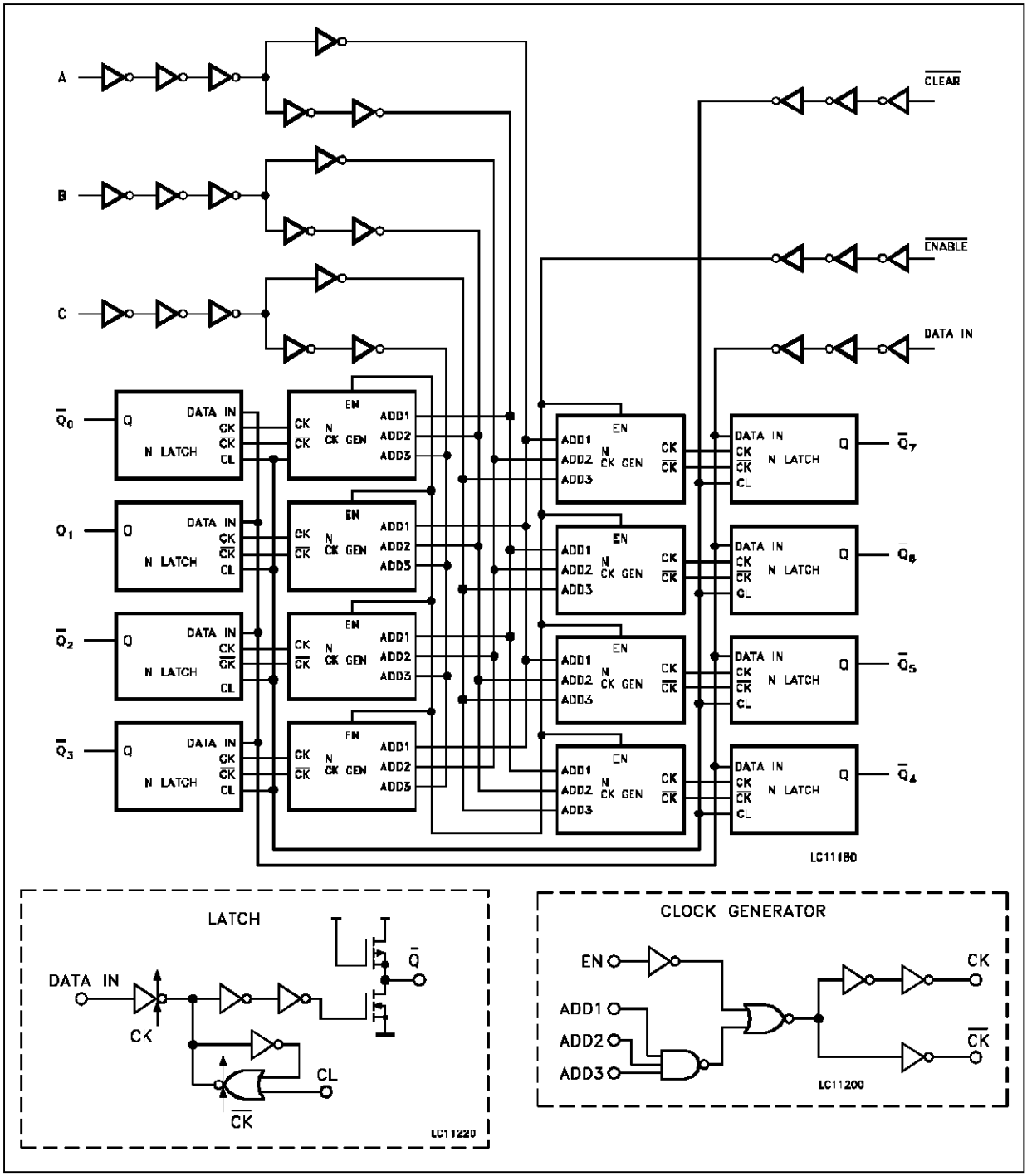


NC =
No Internal
Connection

(inactive) while the address lines are changing. If ENABLE is held high and CLEAR is taken low all eight latches are cleared to the HIGH (OFF) state. If ENABLE is low all latches except the addressed latch will be cleared. The address latch will instead be the complement of the D input,effectively implementing a 3 to 8 line decoder. Internal clamp diodes protect the open drain outputs against over voltages due to inductive loads.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

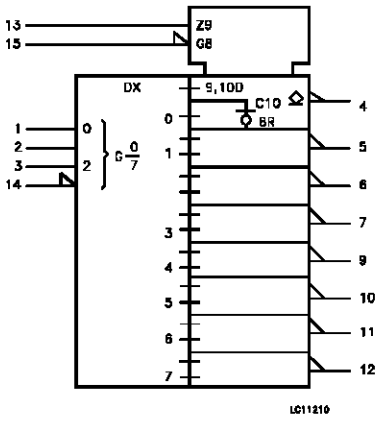
LOGIC DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3	A, B, C	Latch Select
4, 5, 6, 7, 9, 10, 11, 12	$\overline{Q0}$ to $\overline{Q7}$	latch Outputs
13	DATA IN	Data Inputs
14	$\overline{ENABLE}$	Latch Enable Input
15	$\overline{CLEAR}$	Conditional Reset Input
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS		OUTPUTS OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
$\overline{CLEAR}$	$\overline{ENABLE}$			
H	L	$\overline{D}$	QI0	ADDRESSABLE LATCH
H	H	Qi0	Qi0	MEMORY
L	L	$\overline{D}$	H	8-LINE DEMULTIPLEXER
L	H	H	H	CLEAR ALL BITS TO "H"

SELECT INPUTS			LATCH ADDRESSED
C	B	A	
L	L	L	$\overline{Q0}$
L	L	H	$\overline{Q1}$
L	H	L	$\overline{Q2}$
L	H	H	$\overline{Q3}$
H	L	L	$\overline{Q4}$
H	L	H	$\overline{Q5}$
H	H	L	$\overline{Q6}$
H	H	H	$\overline{Q7}$

D: The level at the data input

Qi0: The level before the indicated steady state input conditions were established, (i = 0,1,....,7).

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{DD} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current Per Pin	100	mA
I_{GND}	DC Ground Current	- 800	mA
I_{CC}	DC V_{CC} Current	50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature 10 sec	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value					Unit
		V_{CC} (V)			T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8	V
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1	V
				I_O= 36 mA		0.17	0.26		0.33	
				I_O= 80 mA		0.32	0.40		0.50	
I_{OZ}	Output Leackage Current	5.5	V_I = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND				±5		±50	µA
I_{IN}	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				4		40	µA
			Each Input in Turn: V_{IN} = 0.5 V or 2.4 V All Other Inputs: V_{CC} or GND				3.0		3.9	mA

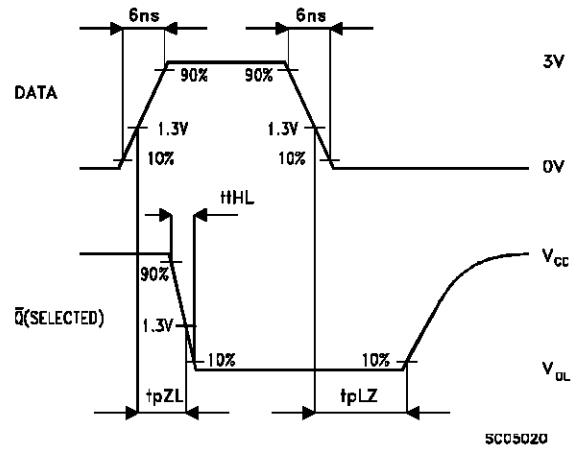
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value					Unit
		V_{CC} (V)	C_L (pF)	R_L (KΩ)	T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
t_{TLH}	Output Transition Time	4.5	50	1		3	6		9	ns
t_{PLZ} t_{PZL}	Propagation Delay Time (DATA - Q)	4.5	50	1		20	31		39	ns
		4.5	150	1		24	37		46	
t_{PLZ} t_{PZL}	Propagation Delay Time (A, B, C - Q)	4.5	50	1		25	39		49	ns
		4.5	150	1		29	45		56	
t_{PLZ} t_{PZL}	Propagation Delay Time (ENABLE - Q)	4.5	50	1		21	33		41	ns
		4.5	150	1		25	39		49	
t_{PLZ} t_{PZL}	Propagation Delay Time (CLEAR - Q)	4.5	50	1		19	30		38	ns
		4.5	150	1		23	36		45	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLEAR}$)	4.5	50	1		7	15		19	ns
$t_{W(L)}$	Minimum Pulse Width ($\overline{ENABLE}$)	4.5	50	1		7	15		19	ns
t_s	Minimum Set-Up Time	4.5	50	1		4	10		13	ns
t_h	Minimum Hold Time	4.5	50	1			5		5	ns
C_{IN}	Input Capacitance					5	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance					96				pF

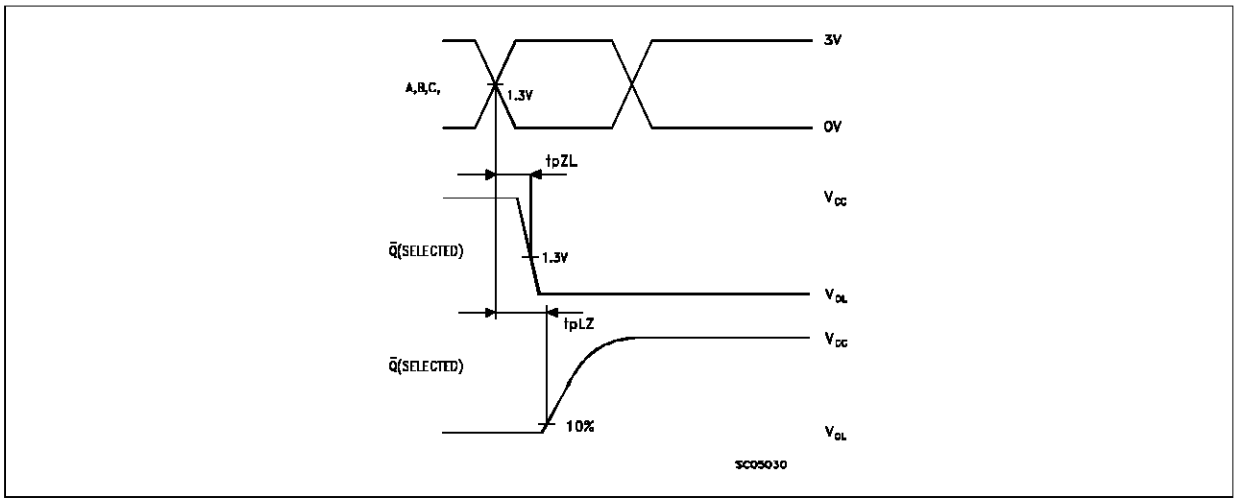
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORMS

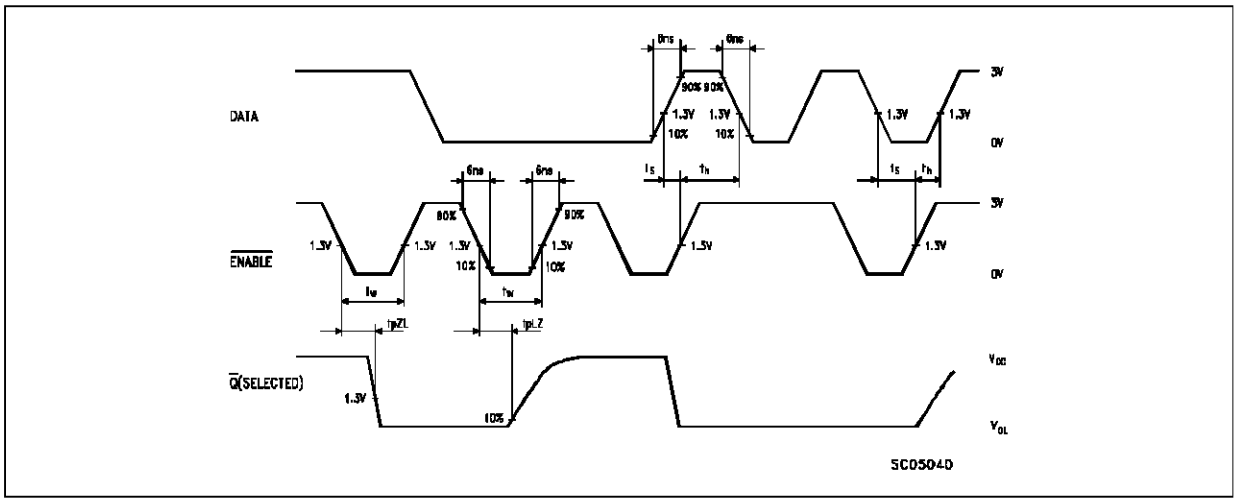
WAVEFORM 1: ($\overline{ENABLE}$ = L, $\overline{CLR}$ = H, A-C= STABLE)



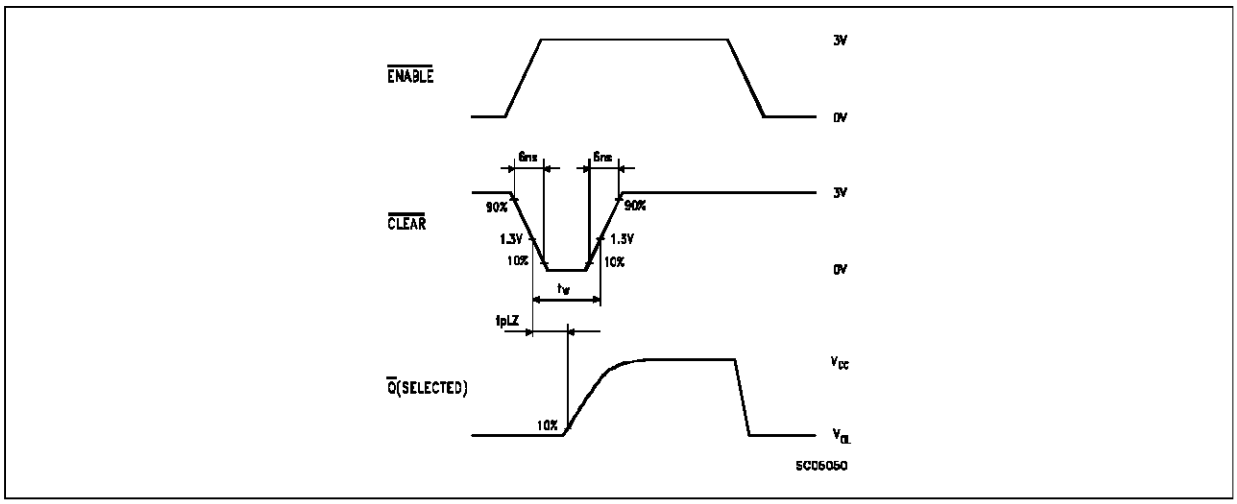
WAVEFORM 2: ($\overline{ENABLE}$ = L)



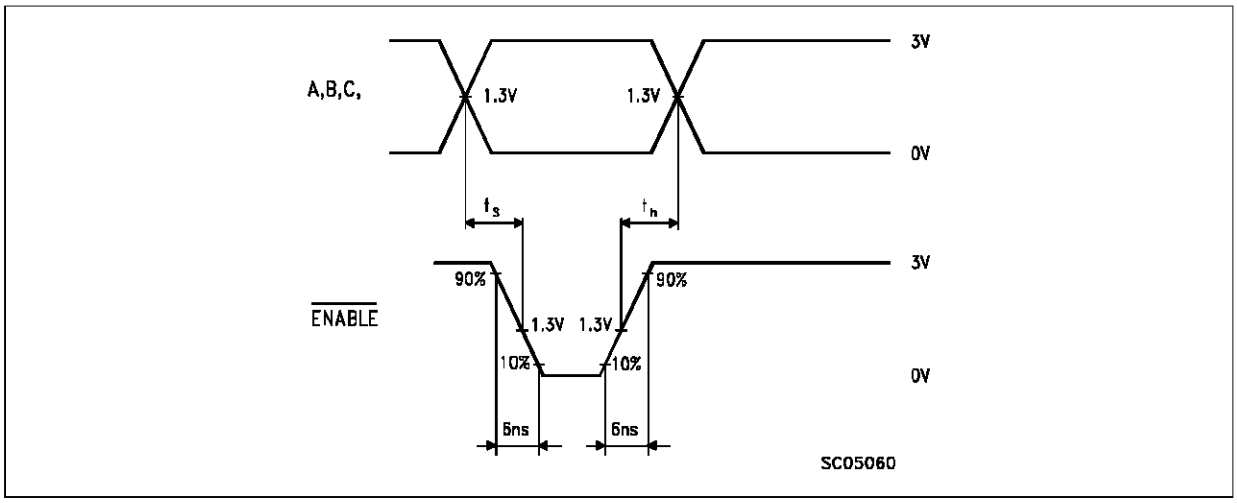
WAVEFORM 3: ($\overline{CLR}$ = H, A-C = STABLE)



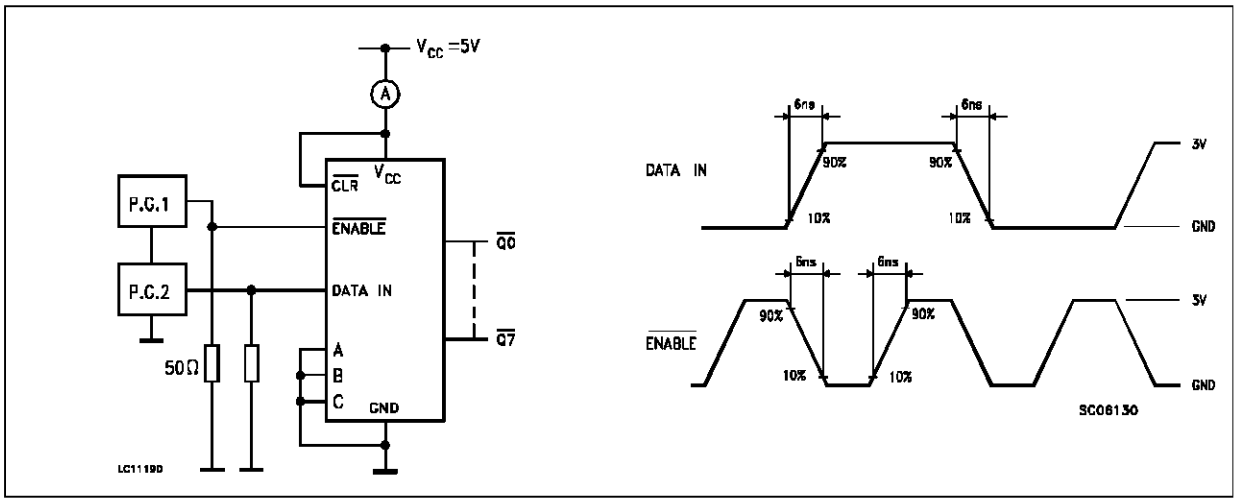
WAVEFORM 4: (D = H, A-C = STABLE)



WAVEFORM 5: ($\overline{CLR}$ = H)

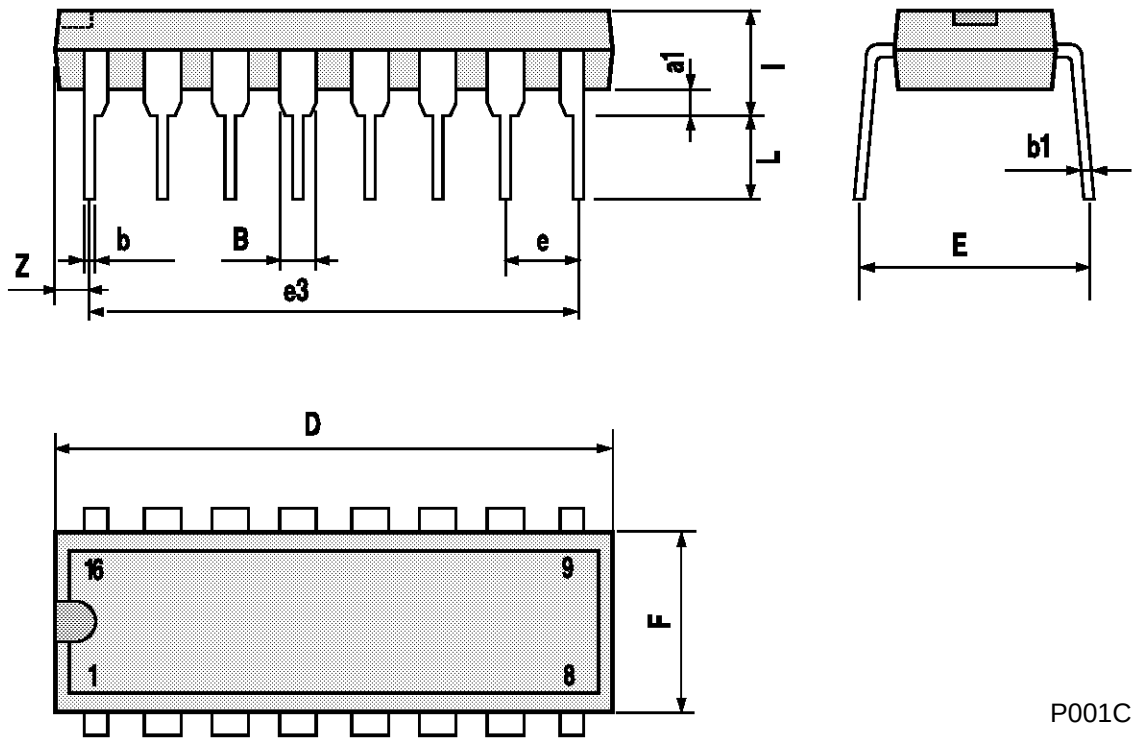


TEST CIRCUIT I_{CC} (Opr.)



Plastic DIP16 (0.25) MECHANICAL DATA

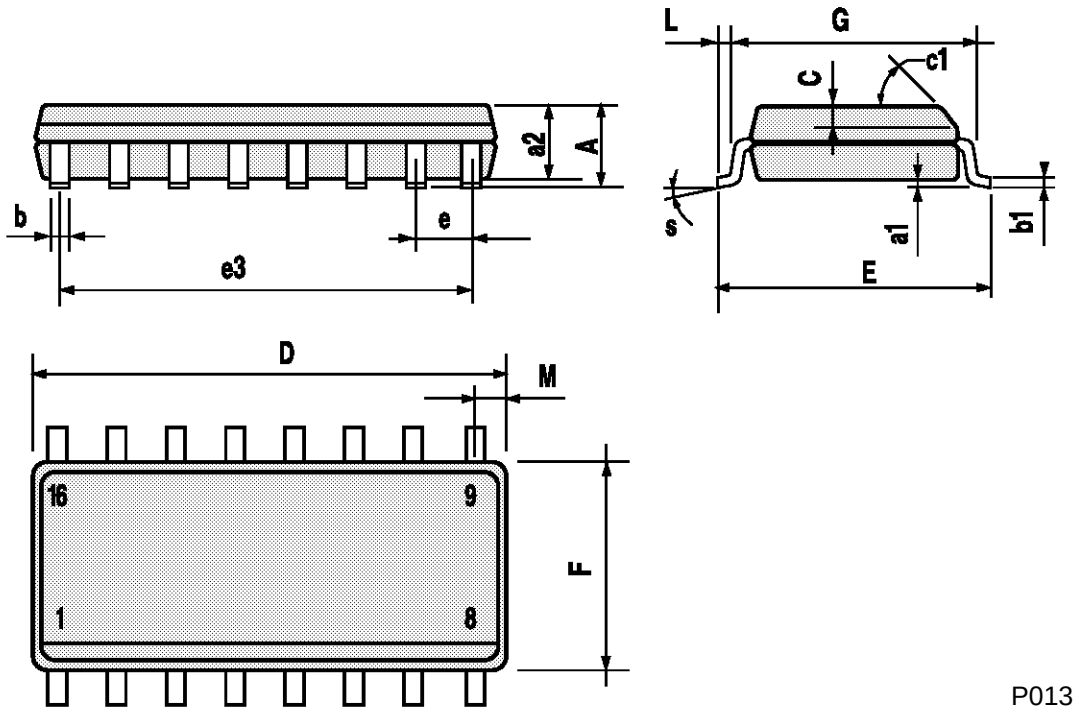
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO16 (Narrow) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



P013H

PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045